Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OUTPUT**
2. **INVERTING INPUT**
3. **NON-INVERTING INPUT**
4. **–VS**
5. **NON-INVERTING INPUT**
6. **INVERTING INPUT**
7. **OUTPUT**
8. **+VS**

**.0133”**

**.067”**

**2 1 8 7**

**6**

**3 4 5**

**648**

**ADI**

**J**

**C**

**DIE ID**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: -VS**

**Mask Ref: 648**

**APPROVED BY: DK DIE SIZE .067” X .113” DATE: 2/8/21**

**MFG: ANALOG DEVICES THICKNESS .026” P/N: AD648**

**DG 10.1.2**

#### Rev B, 7/1